What is claimed is:

1. A method for performing clocked operations in an electronic device, the method comprising the steps of:

performing, in a device, first and second operations responsive to a timing clock having a primary frequency f, wherein the device is capable of performing the operations within X and Y cycles of the clock, respectively, and wherein X cycles of the clock correspond to a time interval T1 with the clock operating at the frequency f, and, accordingly, the device is capable of performing X/Y instances of the second operation within time interval T1 with the clock operating at the frequency f;

generating, during the time interval T1, at least one extra cycle of the clock, to selectively reduce performance time for the first operation; and

masking a certain effect of the at least one extra cycle for the second operation, so that instances of the second operation during the interval T1 remain no greater in number than X/Y.

2. The method of claim 1, wherein a first clock signal has frequency f and a second clock signal has a frequency greater than f, and wherein generating the least one extra cycle comprises selecting, during some of the time T1, the second clock signal for output as the timing clock.

3. The method of claim 2, wherein instances of the second operation are initiated by asserting an operation-initiating control signal in conjunction with asserting the timing clock, and wherein masking the effect of the a least one extra cycle comprises altering timing of the control

signal, so that assertion of the control signal occurs during a different time interval than does assertion of the extra clock cycle.

4. The method of claim 2, wherein a third clock signal has a frequency greater than the frequency of the second clock signal, the method comprising clocking a state machine by the third clock signal.

5. The method of claim 4, wherein initiating the at least one extra cycle includes asserting an extra-clock-cycle-initiating control signal as an input to the state machine.

6. The method of claim 4, the method comprising clocking an output register by the third clock signal.

7. The method of claim 6, wherein initiating the least one extra cycle includes asserting an extra-clock-cycle-initiating control signal as an input to the output register.

8. The method of claim 4, wherein an output register outputs the timing clock responsive to output signals of the state machine.

9. The method of claim 8, wherein the output register outputs a mask signal for masking the certain effect of the extra cycle responsive to output signals of the state machine.

10. An apparatus for performing clocked operations comprising:

first circuitry for performing first and second operations responsive to a timing clock having a primary frequency f, wherein the first circuitry is capable of performing the operations within X and Y cycles of the clock, respectively, and wherein X cycles of the clock correspond to a time interval T1 with the clock operating at the frequency f, and, accordingly, the first circuitry is capable of performing X/Y instances of the second operation within time interval T1 with the clock operating at the frequency f; and

second circuitry for generating, during the time interval T1, at least one extra cycle of the clock, to reduce performance time for the first operation, and for masking an affect of the at least one extra cycle with respect to the second operation, so that instances of the second operation during the interval T1 remain no greater in number than X/Y.

11. The apparatus of claim 10, wherein a first clock signal has frequency f and a second clock signal has a frequency greater than f, and wherein the second circuitry comprises circuitry for selecting, during some of the time T1, the second clock signal for output as the timing clock.

12. The apparatus of claim 11, wherein the first circuitry is operable to initiate instances of the second operation responsive to an operation-initiating-control signal asserted in conjunction with the timing clock, and wherein the second circuitry is operable to alter timing of the control signal, so that assertion of the control signal occurs during a different time interval than does assertion of the extra clock cycle.

13. The apparatus of claim 11, wherein a third clock signal has a frequency greater than the frequency of the second clock signal, and the second circuitry comprises a state machine clocked by the third clock signal.

14. The apparatus of claim 13, wherein the second circuitry is operable to initiate the at least one extra cycle responsive to an extra-clock-cycle-initiating control signal input to the state machine.

15. The apparatus of claim 13, wherein the second circuitry comprises an output register clocked by the third clock signal.

16. The apparatus of claim 15, wherein the second circuitry is operable to initiate the at least one extra cycle responsive to an extra-clock-cycle-initiating control signal input to the output register.

17. The apparatus of claim 13, wherein the second circuitry comprises an output register operable to output the timing clock responsive to output signals of the state machine.

18. The apparatus of claim 17, wherein the output register is operable to output a mask signal for masking the certain effect of the extra cycle responsive to output signals of the state machine.

19. A computer program product for performing clocked operations in an electronic device, wherein the device is operable to perform first and second operations responsive to a timing clock having a primary frequency f, the device being capable of performing the operations within X and Y cycles of the clock, respectively, and wherein X cycles of the clock correspond to a time interval T1 with the clock operating at the frequency f, and, accordingly, the device is capable of performing X/Y instances of the second operation within time interval T1 with the clock operating at the frequency f, the computer program product comprising:

first instructions for generating, during the time interval T1, at least one extra cycle of the clock, to selectively reduce performance time for the first operation; and

second instructions for masking a certain effect of the at least one extra cycle for the second operation, so that instances of the second operation during the interval T1 remain no greater in number than X/Y.

20. The computer program product of claim 19, wherein a first clock signal has frequency f and a second clock signal has a frequency greater than f, and wherein first instructions for generating the least one extra cycle comprise instructions for selecting, during some of the time T1, the second clock signal for output as the timing clock.

21. The computer program product of claim 20, wherein instances of the second operation are initiated in the device by asserting an operation-initiating control signal in conjunction with asserting the timing clock, and wherein the second instructions comprise instructions for altering timing of the control signal, so that assertion of the control signal occurs during a different time interval than does assertion of the extra clock cycle.